[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a method and an apparatus for fabricating a semiconductor device used for dry etching silicon in the fabrication process of a semiconductor device.

[Prior Art]

When dry etching is performed for silicon in the fabrication process of a semiconductor device, an inductively coupled plasma etching apparatus (ICP) and the like have been used to miniaturize a semiconductor element and increase the precision thereof. A characteristic of a dry etching apparatus having a dual power source features separate application of first electric power (hereinafter referred to as source power) for generating a plasma and adjusting the density of the plasma and second electric power (hereinafter referred to as bias power) for drawing ions (etching species) from the plasma into an object to be etched, therefore providing high-accuracy processing properties.

Etching for forming a trench for isolation in a step of forming an isolation is an exemplary dry etching of silicon using the dry etching apparatus having a dual power source. The step of forming an isolation has conventionally used LOCOS (Local Oxidization of Silicon) for forming the isolation by locally oxidizing the silicon substrate masked with a nitride film. However, in such a method, the isolation becomes larger than a desired size, and therefore it is difficult for ensure an active region having a sufficient size as feature sizes have been reduced. Then, STI (Shallow Trench Isolation) has been used as a replacement in which an isolation is formed by forming a trench in a silicon substrate, filling an oxide film in the trench, and then planarizing a surface of the silicon substrate by CMP (Chemical Mechanical Polishing). The foregoing dry etching apparatus having a dual power source is used to form the trench for isolation.

Herein below, a conventional method for forming a trench for isolation in the fabrication of a semiconductor device will be described with reference to FIG. **12**.

FIG. **12** illustrates cross-sectional views of a semiconductor device in the process for fabricating an isolation. FIG. **12(a)** illustrates the state after an oxide film **43** has been formed by oxidizztion of a silicon substrate **42**, a nitride film **44** is formed by the CVD technique and then an isolation pattern is formed using a photolithography technique, **12(b)** illustrates the state immediately after the nitride film and the oxide film are etched using a dry etching technique and thereby a resist is removed, **12(c)** illustrates the state immediately after a silicon substrate is etched using a dry etching technique, and **12(d)** illustrates the state immediately after an oxide film is deposited to fill the trench using the CVD technique, the surface thereof is planarized by CMP and the nitride film is removed by wet etching, respectively. In FIG **12**, **42** denotes a silicon substrate, **43** denotes an oxide film, **44** denotes a nitride film, **45** denotes a photoresist and **46** denotes an oxide film for isolation.

First, the first silicon oxide film **43** is formed on the silicon substrate **43** by thermal oxidation, followed by the nitride film **44** thereon by using a film forming method such as a CVD method. Then, a photoresist **45** is formed as a mask by photolithography (FIG. **12(a)**).

Next, the silicon nitride film **44** and the first silicon oxide film **43** are dry-etched using a dry etching method. Thereafter, ashing and cleaning are performed and the isolation pattern is transferred onto the nitride film **44** (FIG. **12(b)**) by removing the photoresist **45**.

Next, the silicon substrate **42** is placed in the chamber of the dry etching apparatus. Then, the chamber is evacuated till a predetermined degree of vacuum is reached and a gas

required to etch the silicon substrate **42** (hereinafter referred to as a process gas) is introduced into the chamber.

Subsequently, a plasma of the process gas is generated by initiating the application of source gas and then ions in the plasma of the process gas are drawn into the silicon substrate **42** that is an object to be etched. As a result, the ions in the plasma and the silicon substrate **42** react with each other to form a volatile reaction product, and then dry etching is performed by evacuating the chamber. In dry etching using these materials, a mixture of a halogen-containing gas such as Cl_2 or HBr and an oxygen gas is used. Here, since the dry etching step requires processing accuracy as high as required by the processing of a gate electrode due to a reduced size of the isolation, a dry etching apparatus having a dual power source such as an inductively coupled plasma etching apparatus is used in the dry etching step.

Thereafter, cleaning is performed to remove a deposit formed during dry etching of the silicon substrate **42** and thereby a trench for isolation formation in the silicon substrate **42** is formed (FIG. **12(c)**).

Next, in order to lower a surface state in the portions of the surfaces of the trench, the pattern on the silicon substrate (hereafter referred to as a side wall of the trench) is thermally oxidized. Then, an oxide film **46** is deposited by CVD to completely fill the trench. Subsequently, planarization is performed by CMP and the nitride film **44** is removed by wet etching, and thereby the isolation is formed (FIG. **12(d)**).

Here, referring to FIG. **13**, the order of power application in a conventional manner in the case where a dry etching apparatus having a dual power source is used will be described. FIG. **13** illustrates steps of dry etching according to a conventional technique using the apparatus having a dual power source. FIG. **13(a)** illustrates the state immediately after the introduction of a gas (process gas **48**) required to etch the silicon

substrate **47** as an object to be etched into the chamber, FIG. **13(b)** illustrates the state immediately after the application of the source power is initiated, and FIG. **13(c)** illustrates the state immediately after the application of the bias power is initiated.

First, the silicon substrate **47** is placed in a chamber of the dry etching apparatus. Then, the chamber is evacuated till a predetermined degree of vacuum is reached and a gas (process gas **48**) required to etch the silicon substrate **47** is introduced into the chamber (FIG. **13(b)**).

Next, a plasma of the introduced process gas is generated with application of the source gas FIG. **13(b)**). Thereafter, ions **50** in the plasma are drawn into the silicon substrate **47** with application of the bias power (FIG. **13(c)**).

As has been described, the dry etching apparatus having a dual power source is capable of controlling the adjustment of the plasma density independently of the drawing of the ions from the plasma into the object to be etched. Therefore, etching is performed by generating the plasma of the process gas with application of the source power and then drawing the ions from the plasma into the object to be etched with application of the bias power.

[Problems that the Invention is to solve]

With the above-described structure, however, when a silicon substrate dry etched by using the conventional dry etching method, etching may be halted halfway, as shown in FIG. **14**.

Moreover, in dry etching of silicon, the silicon substrate is damaged during the etching, and then the problem that the electric characteristics of the semiconductor device are degraded is caused.

Furthermore, another problem is caused that after a trench is formed for isolation, the wall surfaces of the trench is oxidized by using an oxidation furnace, and therefore cost

for fabricating the semiconductor device is increased disadvantageously by using an oxidation furnace.

A primary object of the present invention is to solve the problem that etching is halted halfway that is caused by dry etching silicon.

[Means for Solving the Problems]

The present inventors have examined the cause of an etching halt in the dry etching method and found the following fact. The found fact will be described with reference to FIG. **8**. FIG. **8** illustrates views showing the mechanism of the etching halt occurring in the conventional dry etching method for silicon. FIG. **8(a)** shows the state immediately after the application of the source power is initiated, FIG. **8(b)** shows the state immediately after active oxygen (oxide radicals **37**) is generated in the plasma by the source power and then an oxide film **39** is formed on a silicon substrate **38** as a film to be etched and FIG. **8(c)** shows the state immediately after the application of the bias power is initiated.

First, the silicon substrate **38** as an object to be etched is placed in the chamber of the dry etching apparatus and the chamber is evacuated till a predetermined degree of vacuum is reached. Then, a gas (process gas) required to etch the silicon substrate **38** is introduced. Thereafter, the source power is applied, whereby the plasma **40** of the process gas is generated (FIG. **8(a)**). Next, the active oxygen (oxygen radicals **37**) in the plasma **40** of the process gas and the silicon substrate **38** that is a film to be etched react with each other to form a thin oxide film **39** on the silicon substrate **38** (FIG. **8(b)**). Thereafter, ions **41** in the plasma of the process gas are drawn into the silicon substrate **38** with application of the bias power (FIG. **8(c)**). However, since the oxide film **39** has been formed on the silicon substrate **38** as an object to be etched, etching hardly proceeds. This is because an etching speed for silicon is about one hundredth of an etching speed for silicon and the etching hardly proceeds.

To verify the mechanism of the etching halt in the conventional dry etching method, the present inventors conducted the following two experiments. First, to verify oxidization of silicon by the source power, the silicon substrate is exposed to the plasma for a predetermined period under the condition described below and the thickness of the silicon oxide film formed on the surface of the silicon substrate was measured. FIG. **9** illustrates the dependence of the thickness of the oxide film of the silicon substrate on the source power application period. The ordinate indicates the thickness of the oxide film of the silicon substrate and the abscissa indicates the source power application period. At this time, an inductively coupled plasma etching apparatus (ICP) was used as a dry etching apparatus having a dual power source under the condition where the source power and the bias power were set at 600 W and 0 W, respectively, a pressure was set at 7 Pa, a Cl_2 gas flow rate was 150 ml/min, and an O_2 gas flow rate was 6 ml/min.

Referring to FIG. **9**, it was found that, if the application of the source power was initiated in the state where the application of the bias power has not been initiated, oxidization at the surface of the silicon substrate proceeds with a lapse of the source power application period.

Next, to verify the relationship between each of the timing of applying the source power and the timing of applying the bias power and a halt in etching performed for silicon, an amount of shaved silicon was measured when dry etching was performed for silicon, while varying the timing of initiating the application of the source power and the timing of initiating the application of the bias power, under the condition described below. Here, the time at which the application of the source power was initiated was used as the reference time and the time at which the application of the bias power was initiated was expressed as a delay time. Also, a sample used in this experiment has been formed in the same manner as in the conventional method shown in FIG. **12**.

At this time, an inductively coupled plasma etching apparatus (ICP) was used as a dry etching apparatus having a dual power source under the condition where the source power and the bias power were set at 600 W and 200 W, respectively, a pressure was 7 Pa, a Cl_2 gas flow rate was 150 ml/min, and an O_2 gas flow rate was 6 ml/min, and the application time was 22 seconds.

FIG. **10** illustrates the dependence of the amount of shaved silicon on the delay time. The ordinate indicates the amount of shaved silicon and the abscissa indicates the delay time. Referring to **10**, it is found that the etching halt occurs in the case where the application of the source power is initiated before the application of the bias power is initiated.

According to the above-described fact, when dry etching is performed using the dry etching apparatus having a dual power source, it is important to prevent oxidization of the silicon that is an object to be etched during dry etching. Thus, in the method using the dry etching apparatus having the dual power source, the application of the bias power is initiated before the application of the source power is initiated. Or the application of the source power is initiated such that an effective value of the source power reaches a predetermined value after an effective value of the bias power reaches another predetermined value. This is shown in an example illustrated in FIG. **11**, in which the ordinate indicates the effective values of the powers applied and the abscissa indicates the time elapsed from the initiation of the application of the powers. As shown in FIG. **11**, as a value predetermined for an effective value of applied power is larger, the time required by the effective value to reach the predetermined value from the initiation of the application thereof becomes longer. Thus, in the case the condition where the source power is higher than the bias power, even if the application of the source power is initiated before the application of the bias power is initiated, it is only required that the effective

value of the source power reaches the second predetermined value after the effective value of the bias power reaches the first predetermined value.

A dry etching method in accordance with the present invention is a dry etching method using a dry etching apparatus having a dual power source capable of independently controlling source power for generating a plasma and bias power for drawing ions from the plasma into a substrate, wherein an object to be etched by the dry etching apparatus includes a silicon substrate or a silicon-containing member formed on the substrate. And the method includes the steps of: placing the substrate in a reaction chamber of the dry etching apparatus; introducing a process gas into the reaction chamber; applying bias power to the substrate; and generating a plasma with the application of source power, in which the application of the bias power is initiated before the oxidation of the surface of the object to be etched proceeds.

According to a dry etching apparatus of the present invention, during dry etching of a silicon-containing member, even slight oxidization of the surface of silicon that is an object to be etched is prevented, and therefore an etching halt can be surely prevented.

Note that it is preferable that the application of the source power is initiated after the application of the bias power is initiated. This is because the surface of can be oxidized even in a short period between a time point when a plasma is generated with the application of the source power to a time point when the etching is started with the application of the bias power.

Alternatively, an arrangement may be made such that an effective value of the bias power reaches a predetermined value before an effective value of the source power reaches another predetermined value. This is because in the case where it takes a long time for the effective value of the source power to reach a predetermined value, for example, even though the application of the bias power and the source power are initiated simultaneously,

the bias power is applied before the source power in the same manner as in the case where the source power is at a higher voltage than the bias power.

This dry etching method can be applied, as can be seen in embodiments that will be described below, in dry etching silicon in a process for forming a trench for isolation and dry etching polysilicon in a process for forming a gate electrode.

Meanwhile, by positively utilizing oxidization of the surface of silicon that is an object to be etched in the dry etching apparatus, the following method for fabricating a semiconductor device can be achieved.

A first method for fabricating a semiconductor device according to the present invention is characterized by the steps of: placing a substrate having a silicon-containing member exposed therefrom in a reaction chamber of the dry etching apparatus; introducing a process gas into the reaction chamber; performing dry etching for the silicon-containing member exposed at the substrate by application of the bias power and the source power; oxidizing a damaged layer generated due to the dry etching; and cleaning the damaged layer to remove it, in which the oxidization of the damaged layer is performed in the reaction chamber by applying not the bias power but only the source power using the plasma.

In the method for fabricating a semiconductor device, oxidization of the surface of the silicon-containing member with the application of the source power is used as a process for oxidizing and removing the damaged layer formed due to etching of the silicon-containing member after etching. Accordingly, it is not required to used a oxidation furnace for performing slight oxidization of the damaged layer, and therefore the fabrication cost can be greatly reduced.

As can be seen in the embodiments described below, this method can be applied, with a silicon-containing member exposed on the substrate used as a silicon substrate, in a

process for forming a trench for isolation in the silicon substrate.

Also, as can be seen in the embodiments described below, the silicon-containing member exposed on the substrate can be used as a polysilicon film formed on the gate insulating film on the substrate and the dry etching process can be applied in a process for forming a gate electrode by etching the polysilicon film.

A second method for fabricating a semiconductor device according to the present invention includes the steps of: placing a silicon substrate in a reaction chamber of a dry etching apparatus, the dry etching apparatus having a dual power source capable of independently controlling source power for generating a plasma in a chamber and bias power for drawing ions from the plasma into a substrate; placing a substrate in the reaction chamber of the dry etching apparatus; introducing a process gas into the reaction chamber; forming a trench for isolation by dry etching part of the silicon substrate with the application of the bias power and the source power; forming an oxide film by oxidization of the surface of the trench for isolation; filling the trench for isolation in the substrate, on which the oxide film is formed, with an insulation film for isolation; and polishing part of the insulation film for isolation by CMP so as to remove it, thereby planarizing the surface of the substrate.

According to the present invention, after the trench for isolation has been formed, oxidization is performed without using an oxidation furnace so as to lower a surface state in the portions of the surfaces of the trench and increases the breakdown voltage of the isolation, and thereby the fabrication cost can be greatly reduced. Note that this method can be used together with the oxidization for removing the damaged layer.

In the case where silicon is oxidized using the dry etching apparatus having a dual power source, a gas containing oxygen may be used as a process gas.

A dry etching apparatus in accordance with the present invention includes bias

power adjusting means for initiating the application of the bias power to the substrate while initializing a timer and continuing the application of the bias power until an effective value of the bias power reaches another predetermined value; and source power adjusting means for initiating the application of the source power when the timer reaches a predetermined time point and continuing the application of the source power until an effective value of the source power reaches another predetermined value.

In the dry etching apparatus in accordance with the present invention, the source power is applied after the bias power is applied at any time by the adjusting means (control means), and therefore an etching halt can be surely prevented.

[Embodiments of the Invention]

(First Embodiment)

Referring to the drawings, a method for fabricating a semiconductor device according to the present invention and an apparatus for fabricating a semiconductor device according to a first embodiment of the present invention will be described. Note that although the fabrication method will be described using dry etching of a silicon substrate in a process for forming an isolation and dry etching of a polysilicon film in a process for forming a gate electrode herein, similar effects can also be expected in other processes for dry etching silicon, a polysilicon film and the like.

FIG. **1** illustrates cross-sectional views showing the individual process steps of the method for fabricating a semiconductor device according to the first embodiment of this invention. In FIG. **1**, **1** denotes a silicon substrate, **2** denotes an oxide film, **3** denotes a nitride film, **4** denotes a resist, and **5** denotes an isolation oxide film. The structure shown here is the same as that of the conventional example.

First, a silicon oxide film **2** is formed on a silicon substrate **1** by thermal oxidation, a silicon nitride film **3** is formed thereon by using a film forming method such as CVD,

and then a desired resist pattern is formed on the silicon nitride film **3** by a photolithography technique (FIG. **1(a)**).

Next, the nitride film **3** and the oxide film **2** are etched using the dry etching technique, ashing and cleaning are performed so that the photoresist **4** is removed, and thereby the isolation pattern is transferred to the nitride film **3** (FIG. **1(b)**). This structure is formed in the same manner as in the conventional example.

The silicon substrate **1** is placed in the chamber of a dry etching apparatus. Then, the chamber is evacuated till a specified degree of vacuum is reached and a gas (process gas) required to etch the silicon substrate **1** is introduced into the chamber. A plasma of the process gas is generated by initiating the application of the bias power and ions in the plasma are drawn into the silicon substrate **1**. Next, another plasma of the introduced process gas is generated by initiating the application of the source power, the process gas and the silicon substrate **1** react with each other to form a volatile reaction product and then dry etching is performed by evacuating the chamber. For example, dry etching is performed using an inductively coupled plasma (ICP) etching apparatus and under the condition where the source power and the bias power are set at 600 W and 200 W, pressure is set at 7 Pa, a Cl_2 gas flow rate is set at 150 ml/min, and an O_2 gas flow rate is set at 6 ml/min. At this time, in order to apply the bias before the application of the source power, the application of the bias power is initiated, e.g., one second before the application of the source power is initiated. Under the condition where the voltage of the source power is higher than that of the bias power, the application of the bias power and the source power are initiated simultaneously so that the effective value of the bias power reaches the set value thereof before the effective value of the source power reaches the set value thereof. For example, the bias power and the source power are simultaneously applied. In this case, since the dry etching of the silicon substrate **1** requires processing accuracy as high as

required by the processing of a gate electrode due to a reduced size of the isolation, the dry etching apparatus having a dual power source such as an inductively coupled plasma (ICP, TCP) etching apparatus, an electron cyclotron resonance (ECR) etcher, a dual-frequency capacitively coupled plasma etcher, or a surface wave plasma (SWP) etcher is used.

Thereafter, the silicon substrate is cleaned such that a deposit formed during dry etching is removed therefrom, whereby the trenches are formed in the silicon substrate **1** (FIG. **1(c)**).

Next, in order to lower a surface state in the portions of the surfaces of the trench, a side wall of the trench is thermally oxidized and then the oxide film **5** is deposited by CVD to fill the trench. Further, planarization is performed by CMP and the oxide film **3** is removed by wet etching, and thereby the isolation is formed (FIG. **1(d)**).

Here, the reason why the application of the source power is initiated before the application of bias power when the dry etching apparatus having a dual power source is used in dry etching the silicon substrate **1** will be described with reference to FIG. **2**. FIG. **2** illustrates steps of dry etching of silicon according to the present invention using the apparatus having a dual power source. FIG. **2(a)** illustrates the state immediately after the introduction of a gas (process gas **6**) required to etch the silicon substrate **1** as an object to be etched into the chamber, FIG. **2(b)** illustrates the state immediately after the application of the bias power is initiated, and FIG. **2(c)** illustrates the state immediately after the application of the source power is initiated.

First, the silicon substrate **1** is placed in a chamber of the dry etching apparatus. Then, the chamber is evacuated till a predetermined degree of vacuum is reached and a gas (process gas **6**) required to etch the silicon substrate **1** is introduced into the chamber (FIG. **2(a)**). Next, a plasma of the introduced process gas is generated with application of the bias gas while ions **8** in the plasma are drawn into the silicon substrate **1** (FIG. **2(b)**).

Thereafter, the application of the source gas is initiated and thereby a plasma **9** of the process gas is formed (FIG. **2(c)**). The application of the bias power is initiated after the application of the source power is initiated in a conventional manner. However, according to the present invention, the application of the source power is initiated after the application of the bias power is initiated. In this manner, the situation associated with the conventional dry etching method, in which active oxygen (oxygen radicals) in the plasma and the silicon substrate as an object to be etched react with each other to form an oxide film. This is because the dry etching method of the present invention accelerates the ions **8** in the plasma before the active oxygen (oxygen radicals) in the plasma and the silicon substrate **1** react with each other such that etching performed for the silicon substrate is thereby initiated. In other words, the active oxygen (oxygen radicals) move randomly but the ions **8** are accelerated by the bias power, and thus the ions **8** reaches the silicon substrate **1** earlier than the active oxygen (oxygen radicals), whereby no oxide film is formed.

(Second Embodiment)

FIG. **3** illustrates cross-sectional views showing the individual process steps of the method for fabricating a semiconductor device according to the second embodiment. In FIG. **3**, **10** denotes a silicon substrate, **11** denotes a gate oxide film, **12** denotes a polysilicon film, and **13** denotes a photoresist.

First, the gate oxide film **11** is formed on the silicon substrate **10** by thermal oxidation, and then the polysilicon film **12** is formed thereon by using a film forming method such as CVD. Then, a desired pattern for the gate electrode is formed from the resist pattern **13** on the polysilicon film **12** by photolithography (FIG. **3(a)**).

The silicon substrate **10** is placed in the chamber of a dry etching apparatus. Then, the chamber is evacuated till a specified degree of vacuum is reached and a gas (process

gas) required to etch the polysilicon film **12** is introduced into the chamber. A plasma of the process gas is generated by initiating the application of the bias power and ions in the plasma are drawn into the silicon substrate **10**. Next, another plasma of the introduced process gas is generated by initiating the application of the source power, the process gas and the polysilicon film **12** react with each other to form a volatile reaction product and then dry etching is performed by evacuating the chamber. For example, dry etching is performed using an inductively coupled plasma (ICP) etching apparatus and under the condition where the source power and the bias power are set at 200 W and 50 W, pressure is set at 4 Pa, a Cl_2 gas flow rate is set at 25 ml/min, and an O_2 gas flow rate is set at 1 ml/min. At this time, in order to apply the bias power before the application of the source power, the application of the bias power is initiated, e.g., one second before the application of the source power is initiated. Under the condition where the voltage of the source power is higher than that of the bias power, the application of the bias power and the source power are initiated such that the effective value of the bias power reaches the set value thereof before the effective value of the source power reaches the set value thereof. For example, the bias power and the source power are simultaneously applied (FIG. **3(b)**). In this case, since the dry etching of the silicon substrate **1** requires processing accuracy as high as required by the processing of a gate electrode due to a reduced size of the isolation, the dry etching apparatus having a dual power source such as an inductively coupled plasma (ICP) etching apparatus is used.

Thereafter, ashing and cleaning are performed to remove the photoresist **13** formed during dry etching of the polysilicon **12**, thereby forming the gate electrode (FIG. **3(c)**).

Conventionally, the application of the bias power is initiated after the application of the source power is initiated. However, the application of the source power is initiated after the application of the bias power is initiated, as in the first embodiment. This method

can be also applied to a method for fabricating the gate electrode.

(Third Embodiment)

Next, a third embodiment of the present invention will be described. FIG. **4** illustrates cross-sectional views showing the individual process steps of the method for fabricating a semiconductor device according to the second embodiment. In FIG. **4**, **14** denotes a silicon substrate, **15** denotes an oxide film, **16** denotes a nitride film, **17** denotes a damaged layer that generates during dry etching of silicon, and **18** denotes an isolation oxide film.

First, the oxide film **15** is formed on the silicon substrate **14** by thermal oxidation, and then the nitride film **16** is formed thereon by using a film forming method such as CVD. Then, a desired pattern for the gate electrode is formed from a photoresist on the nitride film **16** using a photolithography technique.

Next, the nitride film **16** and the oxide film **15** are etched using a dry etching technique and thereby a photoresist is removed. Then, the isolation pattern is transferred onto the nitride **16** (FIG. **4(a)**). This structure is formed in the same manner as in a conventional method.

The silicon substrate **14** is placed in the chamber of a dry etching apparatus. Then, the chamber is evacuated till a specified degree of vacuum is reached and a gas (process gas) required to etch the silicon substrate **14** is introduced into the chamber. A plasma of the process gas is generated, and then the introduced process gas and the silicon substrate **14** react with each other to form a volatile reaction product and then dry etching is performed by evacuating the chamber. In dry etching using these materials, a mixture of a halogen-containing gas such as Cl_2 or HBr and an oxygen gas is used. At this time, the damaged layer **17** is formed on the side wall of the trench as a result of dry etching of the silicon substrate (FIG. **4(b)**).

Subsequently, using the dry etching apparatus, a gas (process gas) required to oxidize the damaged layer **17** is introduced into a chamber. For example, the gas is introduced into the chamber at a gas flow rate of 50 ml/min. Then, only the application of the source power is initiated to generate a plasma from the introduced gas, and then the damage layer **17** is oxidized. For example, using an inductively coupled plasma etching apparatus (ICP), the surface that has been etched under the condition where the source power is 600 W, the bias power is 0 W and pressure is 7Pa is exposed to the plasma.

Thereafter, in order to remove a deposit formed during dry etching of the silicon substrate **14** and the damaged layer **17** on silicon, the substrate is cleaned using a liquid chemical such as HF, whereby trenches for isolation are formed in the silicon substrate **14** from which the damaged layer **17** is removed (FIG. **4(c)**).

Next, in order to lower a surface state in the portions of the surfaces of the trench, the side wall of the trench is thermally oxidized. Then, an oxide film **18** is deposited by CVD to completely fill the trench. Subsequently, planarization is performed using CMP and the nitride film **44** is removed by wet etching, and thereby the isolation is formed (FIG. **4(d)**).

When dry etching is performed for the silicon substrate **14**, the damaged layer **17** is formed on the side wall. The third embodiment, however, has a characteristic that the damage layer **17** is oxidized using the dry etching apparatus having a dual power source and then the substrate is cleaned to remove the damaged layer **17**.

(Fourth Embodiment)

Next, a fourth embodiment of the present invention will be described. FIG. **5** illustrates steps of dry etching according to a conventional technique using the apparatus having a dual power source. In FIG. **5**, **19** denotes a gate oxide film, **21** denotes a polysilicon film, **22** denotes a photoresist, and **23** denotes a damaged layer generated

during dry etching of a polysilicon film.

First, the gate oxide film **20** is formed on the silicon substrate **19** by thermal oxidation, and then the polysilicon film **21** is formed thereon by using a film forming method such as CVD. Then, a desired pattern for the gate electrode is formed from a photoresist **22** using a photolithography technique (FIG. **5(a)**).

The silicon substrate **19** is placed in the chamber of a dry etching apparatus. Then, the chamber is evacuated till a specified degree of vacuum is reached and a gas (process gas) required to etch the polysilicon film **21** is introduced into the chamber. A plasma of the process gas is generated and then the introduced process gas and the polysilicon film **21** react with each other to form a volatile reaction product and then dry etching is performed by evacuating the chamber. In dry etching using these materials, a mixture of a halogen-containing gas such as Cl_2 or HBr and an oxygen gas is used. At this time, the damaged layer **23** is formed on the side wall of the trench as a result of dry etching of the polysilicon film (FIG. **5(b)**).

Subsequently, using the dry etching apparatus, a gas (process gas) required to oxidize the damaged layer **23** is introduced into a chamber. For example, the gas is introduced into the chamber at a gas flow rate of 40 ml/min. Then, only the application of the source power is initiated to generate a plasma from the introduced gas, and then the damage layer **23** is oxidized. For example, using an inductively coupled plasma etching apparatus (ICP), the surface that has been etched under the condition where the source power is 600 W, the bias power is 0 W and pressure is 7Pa is exposed to the plasma.

Next, the photoresist **22** is removed by ashing. Thereafter, in order to remove a deposit formed during dry etching of the polysilicon film **21** and the damaged layer **23** on the side wall of the polysilicon film, the substrate is cleaned using a liquid chemical such as HF, whereby a pattern for the gate electrode is formed in the silicon substrate **19** from

which the damaged layer **23** is removed (FIG. **5(c)**).

When dry etching is performed for the polysilicon film **21**, the damaged layer **23** is formed on the side wall of the gate electrode. The third embodiment, however, has a characteristic that the damage layer **23** is oxidized using the dry etching apparatus having a dual power source and then the substrate is cleaned to remove the damaged layer **23**.

(Fifth Embodiment)

Next, a fifth embodiment of the present invention will be described. FIG. **6** illustrates steps of dry etching according to a conventional technique using the apparatus having a dual power source. In FIG. **6**, **24** denotes a silicon substrate, **25** denotes an oxide film, **26** denotes a nitride film, **27** denotes a side wall of a trench composed of an oxide film, and **28** denotes an oxide film for isolation.

First, the oxide film **25** is formed on the silicon substrate **24** by thermal oxidation, and then the nitride film **26** is formed thereon by using a film forming method such as CVD. Then, a desired pattern for isolation is formed from a photoresist on the nitride **26** using a photolithography technique.

Next, the nitride film **26** and the oxide film **25** are etched using a dry etching technique, ashing and cleaning are performed to remove the photoresist, and thereby the isolation pattern is transferred onto the nitride **26** (FIG. **6(a)**). This structure is formed in the same manner as in a conventional method.

Thereafter, the silicon substrate **24** is etched using a dry etching technique, cleaning is performed to remove a deposit formed during dry etching of the silicon substrate **24** and thereby a trench for isolation formation in the silicon substrate **24** (FIG. **6(b)**).

Next, in order to lower a surface state in the portions of the surfaces of the trench, a side wall of the trench is thermally oxidized. The silicon substrate **24** is placed in a chamber of the dry etching apparatus. Then, the chamber is evacuated till a predetermined

degree of vacuum is reached and a gas (process gas) required to etch the silicon substrate **24** is introduced into the chamber. For example, the gas at O_2 gas flow rate of 60 ml/min is introduced into the chamber. Then, only the application of the source power is initiated to generate a plasma from the introduced gas, the process gas and the silicon substrate **24** react with each other to form an oxide film **27** on a side wall of the trench. For example, using an inductively coupled plasma etching apparatus (ICP), the side wall of the trench is exposed to the plasma and oxidized under the condition where the source power is 600 W, the bias power is 0 W and pressure is 7Pa is exposed to the plasma (FIG. **6(c)**).

Thereafter, an oxide film **28** is deposited by CVD to completely fill the trench. Furthermore, planarization is performed by CMP and the nitride film **24** is removed by wet etching, and thereby the isolation is formed (FIG. **6(d)**).

The fifth embodiment has a characteristic that after dry etching of the silicon substrate **24**, the side wall of the trench is oxidized using the dry etching apparatus having a dual power source and therefore the fabrication cost can be reduced compared with the case in which an oxidation furnace.

(Sixth Embodiment)

FIG. 7 illustrates a dry etching apparatus and a flowchart of the dry etching process according to a sixth embodiment. FIG. 7, **29** denotes a silicon substrate, **30** denotes a process chamber, **31** denotes a process gas, **32** denotes a bias power supply apparatus, **33** denotes a bias power monitor, **34** denotes a timer, **35** denotes source power supply apparatus and **36** denotes a source-power-application instruction signal.

Steps of dry etching using this dry etching apparatus having a dual power source will be described.

The silicon substrate **29** is placed in the process chamber **30** of the dry etching apparatus. The process chamber **30** is evacuated till a predetermined degree of vacuum is

reached and a gas required to etch the silicon substrate **29** (process gas **31**) is introduced into the process chamber **30**. Next, when the pressure of the inside of the process chamber **30** reaches a predetermined value, bias power is applied from the bias power supply apparatus **32**. The bias power is monitored by the bias power monitor **33**. When the set value of the bias power becomes equal to the effective value and the time elapsed from the initiation of the application of the bias power has reached a specified time, the source-power-application instruction signal **36** is transmitted from the bias power monitor **33** to the source power supply apparatus **35**, and thereby the source power is applied from the source power supply apparatus **35**. A plasma from the introduced process gas **31** is generated, the process gas **31** and the silicon substrate **29** react with each other to form a volatile reaction product. Then, the resultant product is vacuumed and thereby etching is performed.

The sixth embodiment has a characteristic that the dry etching apparatus having a dual power source includes a system for initiating the application of the source power after the application of the bias power, so that the source power is not applied before the source power is applied and that this allows dry etching performed such that the silicon surface is not oxidized and no halt is caused halfway in the process.

[Effects of the Invention]

According to the inventive method for fabricating a semiconductor device, during dry etching of silicon, the application of power of a dry etching apparatus having a dual power source, i.e., bias power and source power are initiated in this order. Accordingly, oxidation of a silicon surface can be suppressed and thereby an etching halt due to the oxidation can be surely prevented.

Moreover, according to a damaged layer generated during dry etching of silicon is oxidized using a dry etching apparatus having a dual power source and then the oxidized

layer is cleaned to remove it and thereby damages which occur during etching can be surely and quickly recovered.

Further, according to the inventive method for fabricating a semiconductor device, the side wall of a trench can be oxidized using the dry etching apparatus having a dual power source, and thereby the fabrication cost for semiconductor devices can be prevented from increasing, compared to the case where an oxidation furnace is used.

Still further, according to the inventive method for fabricating a semiconductor device, the dry etching apparatus having a dual power source includes a system for initiating the application of the source power after the application of the bias power, so that the source power is not applied before the source power is applied. Accordingly, dry etching can be performed such that the silicon surface is not oxidized and thereby no etching halt is caused.

[Brief Explanation of the Drawings]

[FIG. 1]

An illustration showing the process steps of a method for fabricating a semiconductor device according to a first embodiment.

[FIG. 2]

An illustration for describing a method for dry etching of silicon according to the first embodiment.

[FIG. 3]

An illustration showing the process steps of a method for fabricating a semiconductor device according to a second embodiment.

[FIG. 4]

An illustration showing the process steps of a method for fabricating a semiconductor device according to a third embodiment.

[FIG. 5]

An illustration showing the process steps of a method for fabricating a semiconductor device according to a fourth embodiment.

[FIG. 6]

An illustration showing the process steps of a method for fabricating a semiconductor device according to a fifth embodiment.

[FIG. 7]

An illustration showing a semiconductor device according to a sixth embodiment.

[FIG. 8]

An illustration for describing an etching halt which occurs during dry etching of silicon.

[FIG. 9]

A graph showing the dependence of the thickness of an oxide film on the source power application period.

[FIG. 10]

A graph showing the dependence of the amount of shaved silicon on a delay time.

[FIG. 11]

A graph showing the dependence of an effective value of a power applied

[FIG. 12]

An illustration showing the process steps of a conventional method for fabricating a semiconductor device.

[FIG. 13]

An illustration for describing a conventional method for dry etching of silicon.

[FIG. 14]

An illustration for describing the problem of an etching halt which occurs in the

conventional method.

[Explanation of the Reference Characters]

1 silicon substrate

2 oxide film

3 nitride film

4 photoresist

5 oxide film for isolation

6 process gas

7 plasma by bias power

8 ions

9 plasma by source power

10 silicon substrate

11 gate oxide film

12 polysilicon film

13 phtotoresist

14 silicon substrate

15 oxide film

16 nitride film

17 damaged layer formed during dry etching of silicon substrate

18 oxide film for isolation

19 silicon substrate

20 gate oxide film

21 polysilicon film

22 photoresist

23 damaged layer formed during dry etching of polysilicon film

24 silicon substrate

25 oxide film

26 nitride film

27 side wall oxide film

28 oxide film for isolation

29 silicon substrate

30 process chamber

31 process gas

32 bias power supply apparatus

33 bias power monitor

34 timer

35 source power supply apparatus

36 source power application instruction signal

37 oxide radicals

38 silicon substrate

39 oxide film

40 plasma by source power

41 ions

42 silicon substrate

43 oxide film

44 nitride film

45 photoresist

46 oxide film for isolation

47 silicon substrate

48 process gas

49 plasma by source power

50 ions

[Name of the Document] Abstract

[Abstract]

[Purpose] To perform dry etching of silicon in a manner to surely prevent an etching halt.

[Solution] An isolation pattern formed from an oxide film **2** and a nitride film **3** on a silicon substrate **1** is formed by a photoresist process step and a dry etching process step. The silicon substrate **1** is placed in a chamber of a dry etching apparatus having a dual power source, which is capable of independently controlling bias power and source power, the chamber is evacuated till a predetermined degree of vacuum is reached and then a process gas is introduced into the chamber. When the application of the source power is initiated after the application of the bias power is initiated so as to generate a plasma at the start of an etching process, an etching halt can be surely prevented. Thereafter, the side wall of a trench is thermally oxidized, followed by filling the trench with an oxide film **5**. Then, the substrate is planarized by CVD and then the nitride film **3** is removed by wet etching to form an isolation.

[Selected Figure] Figure 1